Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **4**
2. **6**
3. **OUT/IN**
4. **7**
5. **5**
6. **IN H**
7. **VEE**
8. **VSS**
9. **C**
10. **B**
11. **A**
12. **3**
13. **0**
14. **1**
15. **2**
16. **VDD**

**.072”**

































**11 10 9 8 7 6**

**5**

**4**

**12**

**13**

**14 15 16 1 2 3**

**.080”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD or FLOAT**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .072” X .080” DATE: 8/7/18**

**MFG: FAIRCHILD THICKNESS .024” P/N: CD4051B**

**DG 10.1.2**

#### Rev B, 7/1